IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of the claims in the application:

1. (Currently Amended) An ultra wide bandwidth timing generator, comprising:

a high frequency clock generation circuit having low phase noise;

a low frequency control generation circuit; ~~and~~

a modulation circuit coupled between the high frequency clock generation circuit and the low frequency control generation circuit[,]; and

a phase accumulator circuit coupled to the low frequency control generation circuit and configured to provide a phase-ramp control signal to the low frequency control generation circuit for fine tuning of the agile timing signal in frequency,

wherein the high frequency clock generation circuit generates a plurality of high frequency clock signals,

the low frequency control generation circuit generates a plurality of low frequency control signals, and

the modulation circuit modulates the high frequency clock signals with the low frequency control signals to produce an agile timing signal at a predetermined frequency and phase by adjustments to at least one of frequency of the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals.

2. (Cancelled)

3. (Cancelled)

4. (Currently Amended) The timing generator of Claim ~~3~~ 1, wherein the phase accumulator circuit is configured to receive a fine frequency control value for generating the phase-ramp control signal.

5. (Original) The timing generator of Claim 1, wherein the low frequency control generation circuit is configured to receive a phase control signal for controlling the agile timing signal in fine time increments.

6. (Original) The timing generator of Claim 1, wherein the high frequency clock generation circuit is configured to receive at least one of a coarse frequency control signal for coarse tuning of the agile timing signal in frequency, and

a fast-modulation control signal for modulating the agile timing signal in frequency.

7. (Original) The timing generator of Claim 1, wherein said plurality of high frequency clock signals comprise a first high frequency sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90° from the first high frequency sinusoidal clock signal.

8. (Original) The timing generator of Claim 7, wherein the plurality of low frequency control signals comprise a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately

90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

9. (Original) The timing generator of Claim 1, wherein the high frequency clock generation circuit is configured to generate a first high frequency sinusoidal clock signal, a second high frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the first through third high frequency sinusoidal clock signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

10. (Original) The timing generator of Claim 9, wherein the low frequency control generation circuit is configured to generate a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated.

11. (Currently Amended) An ultra wide bandwidth timing generation means, comprising:

a high frequency clock generation means having low phase noise for generating a plurality of high frequency clock signals;

a low frequency control generation means for generating a plurality of low frequency control signals; and

a modulation means coupled between the high frequency clock generation means and the low frequency control generation means for modulating the high frequency clock signals with the low frequency control signals to produce an agile timing signal at a predetermined frequency and phase by adjustments to at least one of frequency of the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals,

wherein the high frequency clock generation means receives at least one of

a coarse frequency control signal for coarse tuning of the agile timing signal in frequency, and

a fast-modulation control signal for modulating the agile timing signal in frequency.

12. (Cancelled)

13. (Original) The timing generation means of Claim 11, further comprising:

a phase accumulator means coupled to the low frequency control generation means for providing a phase-ramp control signal to the low frequency control generation means for fine tuning of the agile timing signal in frequency.

14. (Original) The timing generation means of Claim 11, wherein the phase accumulator means receives a fine frequency control value for generating the phase-ramp control signal.

15. (Original) The timing generation means of Claim 11, wherein the low frequency control generation means receives a phase control signal for controlling the agile timing signal in fine time increments.

16. (Cancelled)

17. (Original) The timing generation means of Claim 11, wherein the plurality of high frequency clock signals comprise a first high frequency sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90° from the first high frequency sinusoidal clock signal.

18. (Original) The timing generation means of Claim 17, wherein the plurality of low frequency control signals comprise a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately 90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

19. (Original) The timing generation means of Claim 11, wherein the high frequency clock generation means generates a first high frequency sinusoidal clock signal, a second high

frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the first through third high frequency sinusoidal clock signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

20. (Original) The timing generation means of Claim 11, wherein the low frequency control generation means generates a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated.

21. (Currently Amended) An ultra wide bandwidth timing generation method, comprising:

generating a plurality of high frequency clock signals via a high frequency clock generation circuit having low phase noise;

generating a plurality of low frequency control signals via a low frequency control generation circuit; ~~and~~

modulating, via a modulation circuit coupled between the high frequency clock generation circuit and the low frequency control generation circuit, the high frequency clock signals with the low frequency control signals to produce an agile timing signal at a predetermined frequency and phase by adjustments to at least one of at least one of frequency of

the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals; and

controlling the agile timing signal in fine time increments based on a phase control signal received by the low frequency control generation circuit.

22. (Cancelled)

23. (Original) The method of Claim 21, further comprising:

providing a phase-ramp control signal to the low frequency control generation circuit for fine tuning of the agile timing signal in frequency via a phase accumulator circuit coupled to the low frequency control generation circuit.

24. (Original) The method of Claim 21, further comprising:

generating the phase-ramp control signal based on a fine frequency control value received by the phase accumulator.

25. (Cancelled)

26. (Original) The method of Claim 21, further comprising at least one of the following steps:

tuning of the agile timing signal in frequency based on a coarse frequency control signal received by the high frequency clock generation circuit, and

modulating the agile timing signal in frequency based on a fast-modulation control signal received by the high frequency clock generation circuit.

27. (Original) The method of Claim 21, wherein the step of generating a plurality of high frequency clock signals comprises generating a first high frequency sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90° from the first high frequency sinusoidal clock signal via the high frequency clock generation circuit.

28. (Original) The method of Claim 27, wherein the step of generating the plurality of low frequency control signals comprises generating a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately 90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

29. (Original) The method of Claim 21, wherein the step of generating the plurality of high frequency clock signals comprises generating a first high frequency sinusoidal clock signal, a second high frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the first through third high frequency sinusoidal clock signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

30. (Original) The method of Claim 21, further comprising:

generating a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated, via the low frequency control generation circuit.

31. (Currently Amended) A computer program product comprising a computer storage medium having a computer program code mechanism embedded in the computer storage medium for performing an ultra wide bandwidth timing generation method, the computer program code mechanism performing the steps of:

generating a plurality of high frequency clock signals via a high frequency clock generation circuit having low phase noise;

generating a plurality of low frequency control signals via a low frequency control generation circuit; and

modulating, via a modulation circuit coupled between the high frequency clock generation circuit and the low frequency control generation circuit, the high frequency clock signals with the low frequency control signals to produce an agile timing signal at a predetermined frequency and phase by adjustments to at least one of frequency of the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals.

wherein the step of generating a plurality of high frequency clock signals comprises generating a first high frequency sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90° from the first high frequency sinusoidal clock signal via the high frequency clock generation circuit.

32. (Cancelled)

33. (Original) The computer program product of Claim 31, wherein the computer program code mechanism further performs the steps of:

providing a phase-ramp control signal to the low frequency control generation circuit for fine tuning of the agile timing signal in frequency via a phase accumulator circuit coupled to the low frequency control generation circuit.

34. (Original) The computer program product of Claim 33, wherein the computer program code mechanism further performs the steps of:

generating the phase-ramp control signal based on a fine frequency control value received by the phase accumulator.

35. (Original) The computer program product of Claim 31, wherein the computer program code mechanism further performs the steps of:

controlling the agile timing signal in fine time increments based on a phase control signal received by the low frequency control generation circuit.

36. (Original) The computer program product of Claim 31, wherein the computer program code mechanism further performs at least one the steps of:

tuning of the agile timing signal in frequency based on a coarse frequency control signal received by the high frequency clock generation circuit, and

modulating the agile timing signal in frequency based on a fast-modulation control signal received by the high frequency clock generation circuit.

37. (Cancelled)

38. (Original) The computer program product of Claim 37, wherein the step of generating the plurality of low frequency control signals comprises generating a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately 90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

39. (Original) The computer program product of Claim 31, wherein the step of generating the plurality of high frequency clock signals comprises generating a first high frequency sinusoidal clock signal, a second high frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the first through third high frequency sinusoidal clock

signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

40. (Original) The computer program product of Claim 31, wherein the computer program code mechanism further performs the steps of:

generating a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated, via the low frequency control generation circuit.

41. (Currently Amended) An ultra wide bandwidth (UWB) communications receiver, comprising:

a UWB demodulator configured to demodulate a UWB signal containing received data;

a controller coupled to the UWB demodulator; and

a UWB timing generator coupled to the controller and the UWB demodulator, the UWB timing generator configured to generate an agile timing signal provided to the demodulator, the UWB timing generator including:

a high frequency clock generation circuit having low phase noise;

a low frequency control generation circuit; and

a modulation circuit coupled between the high frequency clock generation circuit and the low frequency control generation circuit,

wherein the high frequency clock generation circuit generates a plurality of high frequency clock signals,

wherein the low frequency control generation circuit generates a plurality of low frequency control signals, ~~and~~

wherein the modulation circuit modulates the high frequency clock signals with the low frequency control signals to produce the agile timing signal provided to the demodulator at a predetermined frequency and phase by adjustments to at least one of frequency of the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals via the controller, and

wherein the plurality of low frequency control signals comprise a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately 90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

42. (Cancelled)

43. (Original) The receiver of Claim 41, further comprising:

a phase accumulator circuit coupled to the low frequency control generation circuit and the controller and configured to provide a phase-ramp control signal to the low frequency control generation circuit for fine tuning of the agile timing signal in frequency.

44. (Original) The receiver of Claim 43, wherein the phase accumulator circuit is configured to receive a fine frequency control value from the controller for generating the phase-ramp control signal.

45. (Original) The receiver of Claim 41, wherein the low frequency control generation circuit is configured to receive a phase control signal from the controller for controlling the agile timing signal in fine time increments.

46. (Original) The receiver of Claim 41, wherein the high frequency clock generation circuit is configured to receive from the controller at least one of a coarse frequency control signal for coarse tuning of the agile timing signal in frequency, and

a fast-modulation control signal for modulating the agile timing signal in frequency.

47. (Original) The receiver of Claim 41, wherein the plurality of high frequency clock signals comprise a first high frequency sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90° from the first high frequency sinusoidal clock signal.

48. (Cancelled)

49. (Original) The receiver of Claim 41, wherein the high frequency clock generation circuit is configured to generate a first high frequency sinusoidal clock signal, a second high

frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the first through third high frequency sinusoidal clock signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

50. (Original) The receiver of Claim 41, wherein the low frequency control generation circuit is configured to generate a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated.

51. (Currently Amended) An ultra wide bandwidth (UWB) communications receiver means, comprising:

a UWB demodulation means for demodulating a UWB signal containing received data;

a control means coupled to the UWB demodulation means; and

a UWB timing generation means coupled to the control means and the UWB demodulation means, for providing an agile timing signal to the UWB demodulation means, the UWB timing generation means including:

a high frequency clock generation means having low phase noise for generating a plurality of high frequency clock signals;

a low frequency control generation means for generating a plurality of low frequency control signals; and

a modulation means coupled between the high frequency clock generation means and the low frequency control generation means for modulating the high frequency clock signals with the low frequency control signals to produce the agile timing signal provided to the demodulation means at a predetermined frequency and phase by adjustments to at least one of frequency of the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals via the control means,

wherein the high frequency clock generation means generates a first high frequency sinusoidal clock signal, a second high frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the first through third high frequency sinusoidal clock signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

52. (Cancelled)

53. (Original) The receiver means of Claim 51, further comprising:

a phase accumulator means coupled to the low frequency control generation means and the control means for providing a phase-ramp control signal to the low frequency control generation means for fine tuning of the agile timing signal in frequency.

54. (Original) The receiver means of Claim 53, wherein the phase accumulator means receives a fine frequency control value from the control means for generating the phase-ramp control signal.

55. (Original) The receiver means of Claim 51, wherein the low frequency control generation means receives a phase control signal from the control means for controlling the agile timing signal in fine time increments.

56. (Original) The receiver means of Claim 51, wherein the high frequency clock generation means receives from the control means at least one of a coarse frequency control signal for coarse tuning of the agile timing signal in frequency, and

a fast-modulation control signal for modulating the agile timing signal in frequency.

57. (Original) The receiver means of Claim 51, wherein the plurality of high frequency clock signals comprise a first high frequency sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90° from the first high frequency sinusoidal clock signal.

58. (Original) The receiver means of Claim 57, wherein the plurality of low frequency control signals comprise a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately 90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

59. (Cancelled)

60. (Original) The receiver means of Claim 51, wherein the low frequency control generation means generates a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated.

61. (Currently Amended) An ultra wide bandwidth (UWB) communications reception method, comprising:

demodulating a UWB signal containing received data via a UWB demodulator coupled to a controller; and

generating an ultra wide bandwidth agile timing signal provided to the UWB demodulator via a timing generation circuit coupled to the UWB demodulator and the controller, including:

generating a plurality of high frequency clock signals via a high frequency clock generation circuit having low phase noise;

generating a plurality of low frequency control signals via a low frequency control generation circuit; and

modulating, via a modulation circuit coupled between the high frequency clock generation circuit and the low frequency control generation circuit, the high frequency clock signals with the low frequency control signals to produce the agile timing signal provided to the

UWB demodulator at a predetermined frequency and phase by adjustments to at least one of at least one of frequency of the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals via the controller,

wherein the step of generating the plurality of low frequency control signals comprises generating a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately 90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

62. (Cancelled)

63. (Original) The method of Claim 61, further comprising:

providing a phase-ramp control signal from the controller to the low frequency control generation circuit for fine tuning of the agile timing signal in frequency via a phase accumulator circuit coupled to the low frequency control generation circuit.

64. (Original) The method of Claim 63, further comprising:

generating the phase-ramp control signal based on a fine frequency control value received by the phase accumulator from the controller.

65. (Original) The method of Claim 61, further comprising:

controlling the agile timing signal in fine time increments based on a phase control signal received by the low frequency control generation circuit from the controller.

66. (Original) The method of Claim 61, further comprising at least one of the following steps:

tuning of the agile timing signal in frequency based on a coarse frequency control signal received by the high frequency clock generation circuit from the controller, and

modulating the agile timing signal in frequency based on a fast-modulation control signal received by the high frequency clock generation circuit from the controller.

67. (Original) The method of Claim 61, wherein the step of generating a plurality of high frequency clock signals comprises generating a first high frequency sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90° from the first high frequency sinusoidal clock signal via the high frequency clock generation circuit.

68. (Cancelled)

69. (Original) The method of Claim 61, wherein the step of generating the plurality of high frequency clock signals comprises generating a first high frequency sinusoidal clock signal, a second high frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the

first through third high frequency sinusoidal clock signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

70. (Original) The method of Claim 61, further comprising:

generating a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated, via the low frequency control generation circuit.

71. (Currently Amended) A computer program product comprising a computer storage medium having a computer program code mechanism embedded in the computer storage medium for performing an ultra wide bandwidth (UWB) communications reception method, the computer program code mechanism performing the steps of:

demodulating a UWB signal containing received data via a UWB demodulator coupled to a controller; and

generating an ultra wide bandwidth agile timing signal provided to the UWB demodulator via a timing generation circuit coupled to the UWB demodulator and the controller, including:

generating a plurality of high frequency clock signals via a high frequency clock generation circuit having low phase noise;

generating a plurality of low frequency control signals via a low frequency control generation circuit; ~~and~~

modulating, via a modulation circuit coupled between the high frequency clock generation circuit and the low frequency control generation circuit, the high frequency clock signals with the low frequency control signals to produce the agile timing signal provided to the UWB demodulator at a predetermined frequency and phase by adjustments to at least one of at least one of frequency of the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals via the controller; and

providing a phase-ramp control signal from the controller to the low frequency control generation circuit for fine tuning of the agile timing signal in frequency via a phase accumulator circuit coupled to the low frequency control generation circuit.

72. (Cancelled)

73. (Cancelled)

74. (Currently Amended) The computer program product of Claim 71 ~~73~~, wherein the computer program code mechanism further performs the steps of:

generating the phase-ramp control signal based on a fine frequency control value received by the phase accumulator from the controller.

75. (Original) The computer program product of Claim 71, wherein the computer program code mechanism further performs the steps of:

controlling the agile timing signal in fine time increments based on a phase control signal received by the low frequency control generation circuit from the controller.

76. (Original) The computer program product of Claim 71, wherein the computer program code mechanism further performs at least one the steps of:

tuning of the agile timing signal in frequency based on a coarse frequency control signal received by the high frequency clock generation circuit from the controller, and

modulating the agile timing signal in frequency based on a fast-modulation control signal received by the high frequency clock generation circuit from the controller.

77. (Original) The computer program product of Claim 71, wherein the step of generating a plurality of high frequency clock signals comprises generating a first high frequency sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90° from the first high frequency sinusoidal clock signal via the high frequency clock generation circuit.

78. (Original) The computer program product of Claim 77, wherein the step of generating the plurality of low frequency control signals comprises generating a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately 90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such

that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

79. (Original) The computer program product of Claim 71, wherein the step of generating the plurality of high frequency clock signals comprises generating a first high frequency sinusoidal clock signal, a second high frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the first through third high frequency sinusoidal clock signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

80. (Original) The computer program product of Claim 71, wherein the computer program code mechanism further performs the steps of:

generating a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated, via the low frequency control generation circuit.

81. (Currently Amended) An ultra wide bandwidth (UWB) communications transmitter, comprising:

a controller;

a UWB modulator coupled to the controller and configured to modulate data to be transmitted as a UWB signal; and

a UWB timing generator coupled to the controller and the UWB modulator and configured to generate an agile timing signal provided to the UWB modulator, the UWB timing generator including:

a high frequency clock generation circuit having low phase noise;

a low frequency control generation circuit; and

a modulation circuit coupled between the high frequency clock generation circuit and the low frequency control generation circuit,

wherein the high frequency clock generation circuit generates a plurality of high frequency clock signals,

the low frequency control generation circuit generates a plurality of low frequency control signals, and

the modulation circuit modulates the high frequency clock signals with the low frequency control signals to produce the agile timing signal provided to the modulator at a predetermined frequency and phase by adjustments to at least one of frequency of the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals via the controller,

<u>wherein the low frequency control generation circuit is configured to receive a phase control signal from the controller for controlling the agile timing signal in fine time increments</u>.

82. (Cancelled)

83. (Original) The transmitter of Claim 81, further comprising:

a phase accumulator circuit coupled to the low frequency control generation circuit and the controller and configured to provide a phase-ramp control signal to the low frequency control generation circuit for fine tuning of the agile timing signal in frequency.

84. (Original) The transmitter of Claim 83, wherein the phase accumulator circuit is configured to receive a fine frequency control value from the controller for generating the phase-ramp control signal.

85. (Cancelled)

86. (Original) The transmitter of Claim 81, wherein the high frequency clock generation circuit is configured to receive from the controller at least one of a coarse frequency control signal for coarse tuning of the agile timing signal in frequency, and

a fast-modulation control signal for modulating the agile timing signal in frequency.

87. (Original) The transmitter of Claim 81, wherein the plurality of high frequency clock signals comprise a first high frequency sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90° from the first high frequency sinusoidal clock signal.

88. (Original) The transmitter of Claim 87, wherein the plurality of low frequency control signals comprise a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately 90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

89. (Original) The transmitter of Claim 87, wherein the high frequency clock generation circuit is configured to generate a first high frequency sinusoidal clock signal, a second high frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the first through third high frequency sinusoidal clock signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

90. (Original) The transmitter of Claim 87, wherein the low frequency control generation circuit is configured to generate a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated.

91. (Currently Amended) An ultra wide bandwidth (UWB) communications transmitter means, comprising:

a control means;

a UWB modulation means coupled to the control means for modulating data to be transmitted as a UWB signal; and

a UWB timing generation means coupled to the control means and the UWB modulation means for generating an agile timing signal provided to the UWB modulation means, the UWB timing generation means including:

a high frequency clock generation means having low phase noise for generating a plurality of high frequency clock signals;

a low frequency control generation means for generating a plurality of low frequency control signals; and

a modulation means coupled between the high frequency clock generation means and the low frequency control generation means for modulating the high frequency clock signals with the low frequency control signals to produce the agile timing signal provided to the UWB modulation means at a predetermined frequency and phase by adjustments to at least one of frequency of the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals via the control means,

wherein the low frequency control generation means generates a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high

frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated.

92. (Cancelled)

93. (Original) The transmitter means of Claim 91, further comprising:

a phase accumulator means coupled to the low frequency control generation means and the control means for providing a phase-ramp control signal to the low frequency control generation means for fine tuning of the agile timing signal in frequency.

94. (Original) The r transmitter means of Claim 93, wherein the phase accumulator means receives a fine frequency control value from the control means for generating the phase-ramp control signal.

95. (Original) The transmitter means of Claim 91, wherein the low frequency control generation means receives a phase control signal from the control means for controlling the agile timing signal in fine time increments.

96. (Original) The transmitter means of Claim 91, wherein the high frequency clock generation means receives from the control means at least one of a coarse frequency control signal for coarse tuning of the agile timing signal in frequency, and

a fast-modulation control signal for modulating the agile timing signal in frequency.

97. (Original) The transmitter means of Claim 91, wherein the plurality of high frequency clock signals comprise a first high frequency sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90o from the first high frequency sinusoidal clock signal.

98. (Original) The transmitter means of Claim 97, wherein the plurality of low frequency control signals comprise a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately 90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

99. (Original) The transmitter means of Claim 91, wherein the high frequency clock generation means generates a first high frequency sinusoidal clock signal, a second high frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the first through third high frequency sinusoidal clock signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

100. (Cancelled)

101. (Currently Amended) An ultra wide bandwidth (UWB) communications transmission method, comprising:

modulating data to be transmitted as a UWB signal via a UWB modulator coupled to a controller; and

generating an ultra wide bandwidth agile timing signal provided to the UWB modulator via a timing generation circuit coupled to the UWB modulator and the controller, including:

generating a plurality of high frequency clock signals via a high frequency clock generation circuit having low phase noise;

generating a plurality of low frequency control signals via a low frequency control generation circuit; and

modulating, via a modulation circuit coupled between the high frequency clock generation circuit and the low frequency control generation circuit, the high frequency clock signals with the low frequency control signals to produce the agile timing signal provided to the UWB modulator at a predetermined frequency and phase by adjustments to at least one of at least one of frequency of the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals via the controller,

wherein the step of generating the plurality of high frequency clock signals comprises generating a first high frequency sinusoidal clock signal, a second high frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the first through third high frequency sinusoidal clock signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

102. (Cancelled)

103. (Original) The method of Claim 101, further comprising:

providing a phase-ramp control signal from the controller to the low frequency control generation circuit for fine tuning of the agile timing signal in frequency via a phase accumulator circuit coupled to the low frequency control generation circuit.

104. (Original) The method of Claim 103, further comprising:

generating the phase-ramp control signal based on a fine frequency control value received by the phase accumulator from the controller.

105. (Original) The method of Claim 101, further comprising:

controlling the agile timing signal in fine time increments based on a phase control signal received by the low frequency control generation circuit from the controller.

106. (Original) The method of Claim 101, further comprising at least one of the following steps:

tuning of the agile timing signal in frequency based on a coarse frequency control signal received by the high frequency clock generation circuit from the controller, and

modulating the agile timing signal in frequency based on a fast-modulation control signal received by the high frequency clock generation circuit from the controller.

107. (Original) The method of Claim 101, wherein the step of generating a plurality of high frequency clock signals comprises generating a first high frequency sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90° from the first high frequency sinusoidal clock signal via the high frequency clock generation circuit.

108. (Original) The method of Claim 107, wherein the step of generating the plurality of low frequency control signals comprises generating a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately 90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

109. (Cancelled)

110. (Original) The method of Claim 101, further comprising:

generating a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated, via the low frequency control generation circuit.

111. (Currently Amended) A computer program product comprising a computer storage medium having a computer program code mechanism embedded in the computer storage medium for performing an ultra wide bandwidth (UWB) communications transmission method, the computer program code mechanism performing the steps of:

modulating data to be transmitted as a UWB signal via a UWB modulator coupled to a controller; and

generating an ultra wide bandwidth agile timing signal provided to the UWB modulator via a timing generation circuit coupled to the UWB modulator and the controller, including:

generating a plurality of high frequency clock signals via a high frequency clock generation circuit having low phase noise;

generating a plurality of low frequency control signals via a low frequency control generation circuit; and

modulating, via a modulation circuit coupled between the high frequency clock generation circuit and the low frequency control generation circuit, the high frequency clock signals with the low frequency control signals to produce the agile timing signal provided to the UWB modulator at a predetermined frequency and phase by adjustments to at least one of at least one of frequency of the low frequency control signals, phase of the low frequency control signals, frequency of the high frequency clock signals, and phase of the high frequency clock signals via the controller; and

providing a phase-ramp control signal from the controller to the low frequency control generation circuit for fine tuning of the agile timing signal in frequency via a phase accumulator circuit coupled to the low frequency control generation circuit.

112. (Cancelled)

113. (Cancelled)

114. (Currently Amended) The computer program product of Claim 111 ~~113~~, wherein the computer program code mechanism further performs the steps of:

generating the phase-ramp control signal based on a fine frequency control value received by the phase accumulator from the controller.

115. (Original) The computer program product of Claim 111, wherein the computer program code mechanism further performs the steps of:

controlling the agile timing signal in fine time increments based on a phase control signal received by the low frequency control generation circuit from the controller.

116. (Original) The computer program product of Claim 111, wherein the computer program code mechanism further performs at least one the steps of:

tuning of the agile timing signal in frequency based on a coarse frequency control signal received by the high frequency clock generation circuit from the controller, and

modulating the agile timing signal in frequency based on a fast-modulation control signal received by the high frequency clock generation circuit from the controller.

117. (Original) The computer program product of Claim 111, wherein the step of generating a plurality of high frequency clock signals comprises generating a first high frequency

sinusoidal clock signal and second high frequency sinusoidal clock signal shifted in phase by 90° from the first high frequency sinusoidal clock signal via the high frequency clock generation circuit.

118. (Original) The computer program product of Claim 117, wherein the step of generating the plurality of low frequency control signals comprises generating a first low frequency approximately sinusoidal control signal and a second low frequency approximately sinusoidal control signal shifted in phase by approximately 90° from the first low frequency sinusoidal control signal for controlling a magnitude, in the range of +1 to -1, of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal, such that a sum of the first high frequency sinusoidal clock signal and the second high frequency sinusoidal clock signal produces the agile timing signal with a predetermined arbitrary phase between 0 and 2π.

119. (Original) The computer program product of Claim 111, wherein the step of generating the plurality of high frequency clock signals comprises generating a first high frequency sinusoidal clock signal, a second high frequency sinusoidal clock signal and a third high frequency sinusoidal clock signal having approximately 0°, 120° and 240° phase relationships, respectively, such that the first through third high frequency sinusoidal clock signals can be positively weighted in the range of 0 to 1 and summed to produce the agile timing signal with any arbitrary phase.

120. (Original) The computer program product of Claim 111, wherein the computer program code mechanism further performs the steps of:

generating a first low frequency control signal, a second low frequency control signal and a third low frequency control signal to control the amplitudes of the first high frequency sinusoidal clock signal, the second high frequency sinusoidal clock signal and the third high frequency sinusoidal clock signal, respectively, such that the agile timing signal with an arbitrary phase can be generated, via the low frequency control generation circuit.